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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,776	10/30/2003	Frederick A. Perner	100111474-7	8879

7590 11/02/2004

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EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,776	PERNER ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-11 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-11 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Preliminary Amendment filed on October 30, 2003 has been entered.

2. Claims 2-5, 12-16 are cancelled.

3. Claims 1, 6-11, 17-20 are present for examination.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 6-8, 10, 17, 19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Gallagher et al. (U.S. Patent No. 5,640,343).

Regarding claim 1, Gallagher et al. discloses, in FIG. 2, a data storage device comprising:

an array of resistive memory cells having rows and columns;

a set of diodes, each electrically connected in series to a resistor in each of resistive memory cells in the array;

a plurality of word lines extending along the rows of the array (1-3);

a plurality of bit lines extending along the columns of the array (4-6);

a first selected resistive memory cell in the array (70), wherein the first selected resistive memory cell is positioned between a first word line (1) in the plurality of word lines and a first bit line (4) in the plurality of bit lines; and

a circuit (51s and 53s) electrically connected to the array and capable to applying a first voltage (Vw) to the first word line, a second voltage (Vb) to a first selected bit line, and a third voltage (Vw) to at least one of second word line in the plurality of word lines and a second bit line in the plurality of bit lines (to WL 2, 3) (See FIG. 3 for time periods of Write 1 and Write 0).

Regarding claims 6-8, Gallagher et al. also discloses that the circuit is capable of writing to the first selected resistive memory cell by applying sufficient energy to the first word line and the first bit line to transform the first selected resistive memory cell from a first resistance state to a second resistance state; sensing a current flowing through the first selected resistive memory cell; values of the first voltage and the third voltage are substantially equal

(See column 7, line 55 to column 8, line 51, and FIG. 3 for time periods of Write 1 and Write 0 with values of Iw and Ib applied).

Regarding claims 10, 17, 19, 20, they encompass the same scope of invention as to that of claims 1, 6-8 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

6. Claims 1, 9, 10, 18 rejected under 35 U.S.C. 102(e) as being anticipated by Sharma et al. (PGPub. 2003/0185038)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C.

102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1 and 9, Sharma et al. disclose a data storage device comprising an array of resistive memory cells having rows and columns; a set of diodes, each electrically connected in series to a resistor in each of resistive memory cells in the array; a plurality of word lines extending along the rows of the array (1-3); a plurality of bit lines extending along the columns of the array (4-6) (see FIG. 1); a first selected resistive memory cell in the array (42, see FIG. 5), wherein the first selected resistive memory cell is positioned between a first word line (26, see FIG. 5) in the plurality of word lines and a first bit line (22, see FIG. 5) in the plurality of bit lines; and a circuit (all transistors in FIG. 5) electrically connected to the array and capable to applying a first voltage (Vrd) to the first word line, a second voltage (virtually ground) to a first selected bit line, and grounding least one of second word line in the plurality of word lines and a second bit line in the plurality of bit lines (to bit lines 20 and 24).

(See paragraphs [0054] and [0055])

Regarding claims 10 and 18, they encompass the same scope of invention as to that of claims 1, 9 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VTN
October 31, 2004

VanThu Nguyen
Primary Examiner
Art Unit 2824